Version with Markings to Show Changes Made:

In the Claims:

Claim 1 (amended). A printed circuit board configuration with a multipole plug-in connector, comprising:

a board having at least two layers, each one of said at least two layers having an edge region and a first of said two layers being an outermost layer and a second of said two layers being directly adjacent said outermost layer;

a plurality of signal conductor tracks disposed in said edge region of [one of] said outermost [layers] layer;

a plurality of plug pins, each one of said plurality of said plug pins fixed to a respective one of said plurality of said signal conductor tracks in a direction parallel to said one of said layers;

a plurality of ground conductor tracks disposed on said [one of said layers and assigned to said plurality of said signal conductor tracks] outermost layer;

a side-to-side configuration in which said plurality of said signal conductor tracks and said plurality of said ground conductor tracks are alternatingly disposed on said [one of said layers] outermost layer, and in which said plurality of

said signal conductor tracks run essentially parallel with respect to said plurality of said ground conductor tracks;

at least one filter capacitor connected between a respective one of said plurality of said signal conductor tracks and a respective one of said plurality of said ground conductor tracks; and

a ground shielding surface disposed on [an] said directly adjacent [one of said layers] layer and covering said side-to-side configuration.

Claim 7 (amended). The printed circuit board configuration according to claim 1, wherein:

[said one of said layers defines a first outer board layer, said another one of said layers defines an inner board layer,] said at least two layers includes a second [outer] outermost board layer remote from said first [outer] outermost board layer, said second [outer] outermost board layer [has] having an outer edge region; and

said plurality of said signal conductor tracks defines a first plurality of signal conductor tracks, said plurality of said plug pins defines a first plurality of plug pins, said plurality of said ground conductor tracks defines a first

plurality of ground conductor tracks, and said side-to-side configuration defines a first side-to-side configuration, the printed circuit board configuration including:

a second plurality of signal conductor tracks disposed in said edge region of said second [outer] outermost board layer;

a second plurality of plug pins, each one of said second plurality of said plug pins fixed to a respective one of said second plurality of said signal conductor tracks in a direction parallel to said second [outer] outermost board layer;

a second plurality of ground conductor tracks disposed on said second [outer] outermost board layer and assigned to said second plurality of said signal conductor tracks; and

a second side-to-side configuration in which said second plurality of said signal conductor tracks and said second plurality of said ground conductor tracks are alternatingly disposed on said second [outer] outermost board layer, and in which said second plurality of said signal conductor tracks run essentially parallel with respect to said second plurality of said ground conductor tracks.

Add the Following Claims:

--8. The printed circuit board configuration according to claim 1, wherein said board has only two layers.--

--9. A printed circuit board configuration with a multipole plug-in connector, comprising:

a board having at least three layers, each one of said at least three layers having an edge region; a first of said at least three layers defines a first outer board layer, a second of said at least three layers defines an inner board layer, and a third of said at least three layers includes a second outer board layer remote from said first outer board layer;
a plurality of signal conductor tracks disposed in said edge region of one of said layers;

a plurality of plug pins, each one of said plurality of said plug pins fixed to a respective one of said plurality of said signal conductor tracks in a direction parallel to said one of said layers;

a plurality of ground conductor tracks disposed on said one of said layers and assigned to said plurality of said signal conductor tracks;

a side-to-side configuration in which said plurality of said signal conductor tracks and said plurality of said ground conductor tracks are alternatingly disposed on said one of said layers, and in which said plurality of said signal conductor tracks run essentially parallel with respect to said plurality of said ground conductor tracks;

at least one filter capacitor connected between a respective one of said plurality of said signal conductor tracks and a respective one of said plurality of said ground conductor tracks;

a ground shielding surface disposed on an adjacent one of said layers and covering said side-to-side configuration;

said plurality of said signal conductor tracks defining a first plurality of signal conductor tracks, said plurality of said plug pins defining a first plurality of plug pins, said plurality of said ground conductor tracks defining a first plurality of ground conductor tracks, and said side-to-side configuration defining a first side-to-side configuration, the printed circuit board configuration including:

a second plurality of signal conductor tracks disposed in said edge region of said second outer board layer;

a second plurality of plug pins, each one of said second plurality of said plug pins fixed to a respective one of said second plurality of said signal conductor tracks in a direction parallel to said second outer board layer;

a second plurality of ground conductor tracks disposed on said second outer board layer and assigned to said second plurality of said signal conductor tracks; and

a second side-to-side configuration in which said second plurality of said signal conductor tracks and said second plurality of said ground conductor tracks are alternatingly disposed on said second outer board layer, and in which said second plurality of said signal conductor tracks run essentially parallel with respect to said second plurality of said ground conductor tracks.--